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12-07-01

Patent
Attorney's Docket No. 027260-468

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Michio KOMODA et al.	)	Group Art Unit: 2123
	)	
Application No.: 09/879,197	)	Examiner: Unassigned
	)	
Filed: June 13, 2001	)	
	)	
For: DELAY TIME ESTIMATION METHOD AND RECORDING...	)	
	)	

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is an Information Disclosure Statement and accompanying form PTO-1449 for the above-identified patent application.

[X] No additional fee for submission of an IDS is required.

[ ] The fee of $180.00 (126) as set forth in 37 C.F.R. § 1.17(p) is also enclosed.

[ ] A certification under 37 C.F.R. § 1.97(e) is also enclosed.

[ ] A certification under 37 C.F.R. § 1.97(e), and the fee of $180.00 (126) as set forth in 37 C.F.R. § 1.17(p) are also enclosed.

[ ] Charge $_____ to Deposit Account No. 02-4800 for the fee due.

[ ] A check in the amount of $_____ is enclosed for the fee due.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Ellen Marcie Emas
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Date: September 17, 2001

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: September 17, 2001

Sir:

In accordance with the duty of disclosure as set forth in 37 C.F.R. § 1.56, Applicant hereby submits the following information in conformance with 37 C.F.R. §§ 1.97 and 1.98. Pursuant to 37 C.F.R. § 1.98, a copy of each of the documents cited is enclosed.

1. "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation", Proc. IEEE International Conference on Computer-Aided Design, 1989.

2. "A Gate-Delay Model for High-Speed CMOS Circuits", Proc. 31st ACM/IEEE Design Automation Conference, 1994.

3. JP-A 9-211087

4. U.S. Application No. 09/878,352, Michio KOMODA et al., June 12, 2001

The documents are being submitted within 3 months of the filing or entry of the national stage of this application or before the first Office Action on the merits, whichever is later, therefore no fee or certification is required under 37 C.F.R. § 1.97(b).

To assist the Examiner, the documents are listed on the attached form PTO-1449. It is respectfully requested that an Examiner initialed copy of this form be returned to the undersigned.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
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Date: September 17, 2001

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

ATTORNEY'S DKT NO.	APPLICATION NO.
027260-468	09/879,197
APPLICANT: Michio KOMODA et al.	
FILING DATE: June 13, 2001	GROUP: 2123

U.S. PATENT DOCUMENTS

Examiner Initials	U.S. Patent Document Number	U.S. Patent Document Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication (MM-DD-YYYY)

FOREIGN PATENT DOCUMENTS

Examiner Initials	Foreign Patent Document Number	Foreign Patent Document Kind Code (if known)	Country	Date of Publication (MM-DD-YYYY)	Translation Yes	Translation no
	JP-A 9-211087		JAPAN	08-15-1997	Abst	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	"Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation", Proc. IEEE International Conference on Computer Aided Design, 1989, Peter R. O'BRIEN et al., IEEE
	"A Gate-Delay Model for High-Speed CMOS Circuits", Proc. 31st ACM/IEEE Design Automation Conference, 1994, Florentin DARTU et al., The University of Texas at Austin, Austin, Texas 78712
	U.S. Application No. 09/878,352, Michio KOMODA et al., " Method of Producing Load for Delay Time Calculation and Recording Medium", June 12, 2001

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. SEND TO: Assistant Commissioner for Patents, Washington, D.C. 20231.